IMPLEMENTATION AND VERIFICATION OF DUAL PORT SRAM USING VERILOG

[1]Dr.P.SREENIVASULU, [2]B.SRI LAKSHMI, [3]G.SIVA GOVINDU, [4]CHUKKALURU MANASA, [5]CHINTHAPALLI KEERTHI, [6]DHANAKAYALA MALLAPPAGARI MALLISWARI

[1]PROFESSOR, DEPT OF ECE, Dr.SAMUEL GEORGE INSTITUTE OF ENGINEERING AND TECHNOLOGY, MARKAPUR

[2,3,4,5,6]U.G STUDENT, DEPT OF ECE, Dr.SAMUEL GEORGE INSTITUTE OF ENGINEERING AND TECHNOLOGY, MARKAPUR

ABSTRACT

A multiport memory cell using a dual-port memory structure enables simultaneous access for multi-processor applications. This is achieved through two-pass transistors, paired bit lines, and a word line, allowing access to the SRAM cell via specific word and bit lines. Unlike single-port SRAM, which can only access one memory cell per clock pulse, dual-port RAM supports concurrent read and write operations at different addresses, overcoming this limitation. Dual-port RAM enhances efficiency by allowing each processor to operate at the same clock frequency, eliminating access constraints between the two ports.

INTRODUCTION

System-On-Chip (SoC) systems primarily rely on memories, with SRAM being a popular choice due to its robustness, high speed, and ease of integration into logic circuits. However, SRAM has the disadvantage of occupying more area, affecting power consumption and yield. Dynamic RAM (DRAM) requires less area but needs constant refreshing to retain data, while SRAM does not need refreshing but is slower and occupies more area for the same memory size. Dual-port RAM overcomes the limitations of single-port RAM by allowing simultaneous data access at different addresses, thus improving speed and efficiency. In dual-port memory systems, single or multi-bank configurations are used, with multi-bank systems employing a single decoder and control to manage multiple arrays. The proposed design utilizes single-bank architecture for simplicity and efficient analysis. Dual-port SRAM improves memory access efficiency by allowing concurrent read/write operations at different addresses, which can operate at different clock frequencies, enhancing performance in multi-processor applications.

LITERATURE SURVEY

A new P-MBIST (Programmable Built-In Self-Test) approach is proposed, merging FSM and Microcode architecture through the use of macro-commands. This hybrid design leverages macro-commands to select the test algorithm and encoding techniques for MARCH elements, but replaces state machines with microcode clusters to control read/write operations and test data injection. The EDA industry

is increasingly focused on maintenance methodologies to enhance software quality, which directly impacts customer satisfaction. Monitoring and detecting post-development software errors are crucial. The TMB Validator experiments show its ability to verify controller features and work with various memory fault models. The current March Algorithm with 22 N is inefficient for full SRAM diagnosis. The proposed scheme improves efficiency by reducing circuit size, test data application, and testing time. As embedded recollections in System-on-Chip (SoC) dominate over 90% of the area, SRAM performance and yield are crucial. While SRAM is costlier and less dense than DRAM, programmable BIST approaches that offer flexible memory testing are desirable but may result in excessive area costs. Prior BIST solutions allow test algorithm and data background programmability at low area cost, but no prior work has addressed programming the address sequence for the test.

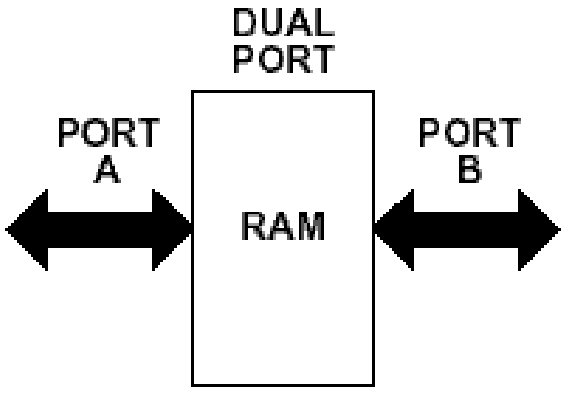
EXISTING SYSTEM

To accommodate a broad range of vendors while providing designers with flexibility, five basic RAM interfaces have been defined: two single-port and three dual-port types. The first is an asynchronous single-port RAM with one address bus, a write enable, and separate data-in and data-out buses. The second type is a synchronous single-port RAM, which includes an additional clock input.

PROPOSED SYSTEM

Single-port memories have only one port for reading and writing data, with separate input and output connections and a single address input, limiting access to one operation at a time. To address this limitation, multi-port memories were designed, featuring multiple address inputs and corresponding data inputs and outputs, allowing for concurrent operations. Dual-port memory is the most common form of multi-port memory. While multi-port memories consume more area and cost due to additional address decoders, data multiplexers, and wiring, they are valuable for high-speed and high-performance applications. In scenarios where multiple subsystems need access to memory, single-port memory requires multiplexing of data and address lines, which can create bottlenecks and data loss. The solution is multi-port memory, where each subsystem has separate access ports, avoiding data contention. However, asynchronous dual-port memory can experience delayed responses or unpredictable results if both subsystems attempt write operations simultaneously, which can be mitigated with additional circuits to manage contention and timing.

SYSTEM ARCHITECTURE



Memory devices and systems are becoming increasingly complex to meet growing information processing demands, particularly in multiprocessor applications

where centralized data storage is essential. This requires innovative solutions for consolidating system information across multiple buses. Additionally, power efficiency is a key consideration, especially for portable systems that rely on rechargeable batteries. For systems with infrequent but large memory transfers, shared mass storage devices like floppy disks or networked hard drives may suffice. However, for frequent, low-density data access, such devices are impractical due to slow data retrieval speeds. The DS1609 Dual Port RAM addresses this challenge by enabling high-frequency, low-volume data storage and retrieval between asynchronous systems. Operating at voltages as low as 2.5 volts, it is well-suited for portable applications with limited power availability.

APPLICATIONS

Co-processor architecture is commonly utilized in various applications, including wireless systems, audio and video processing, and control systems, to enhance overall system performance by offloading specific tasks and enabling faster processing.

FUTURE SCOPE

The implementation and verification of Dual-Port SRAM using Verilog provide an efficient way to handle simultaneous read and write operations, improving data access speed and performance. Future work could explore optimizing the memory architecture to reduce area and power consumption, as well as integrating advanced techniques like multi-level cache management or error correction. Additionally, the design can be expanded to support higher memory capacities and faster access speeds to meet the demands of modern applications such as high-performance computing and real-time systems.

CONCLUSION

The implementation of dual-port memory allows for concurrent read and write operations, enhancing performance. However, the main drawback is the increased area required for its implementation. The dual-port memory has been successfully implemented and tested using Xilinx ISE software.

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